

# SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 – MARCH 1985 – REVISED MARCH 1988

## 'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

## 'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

## description

### SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level ( $\overline{CS}$ ) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

### SN54LS674, SN74LS674

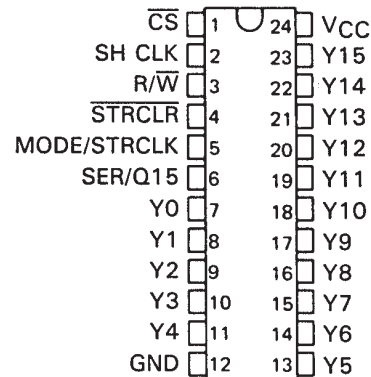
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

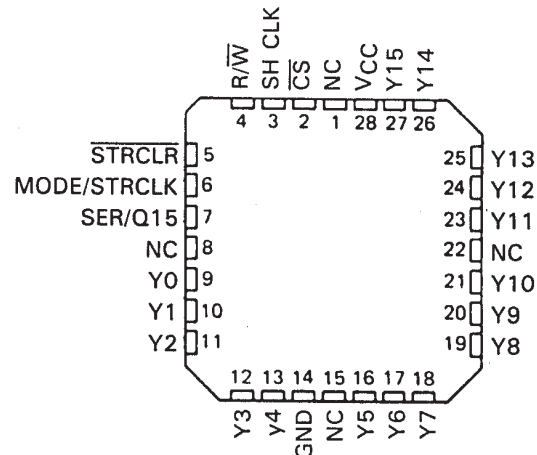
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

### SN54LS673 . . . J OR W PACKAGE SN74LS673 . . . DW OR N PACKAGE (TOP VIEW)



### SN54LS673 . . . FK PACKAGE (TOP VIEW)

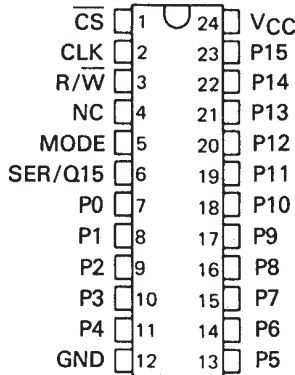


NC—No internal connection

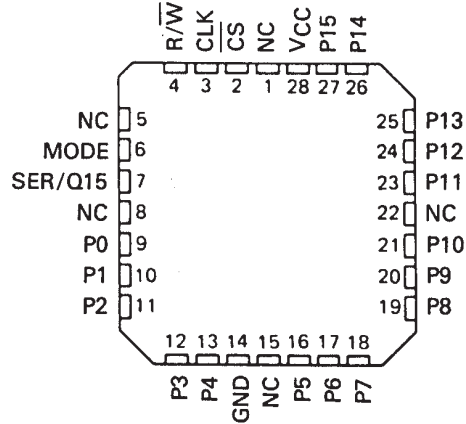
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SN54LS674 . . . J OR W PACKAGE  
SN74LS674 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54LS674 . . . FK PACKAGE  
(TOP VIEW)



'LS673  
FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
CS	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)  
L = low level (steady state)  
↑ = transition from low to high level  
↓ = transition from high to low level  
X = irrelevant (any input including transitions)  
Z = high impedance, input mode  
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.  
Q15 = present content of 15th bit of the shift register  
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.  
P15 = level of input P15

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logic symbols†

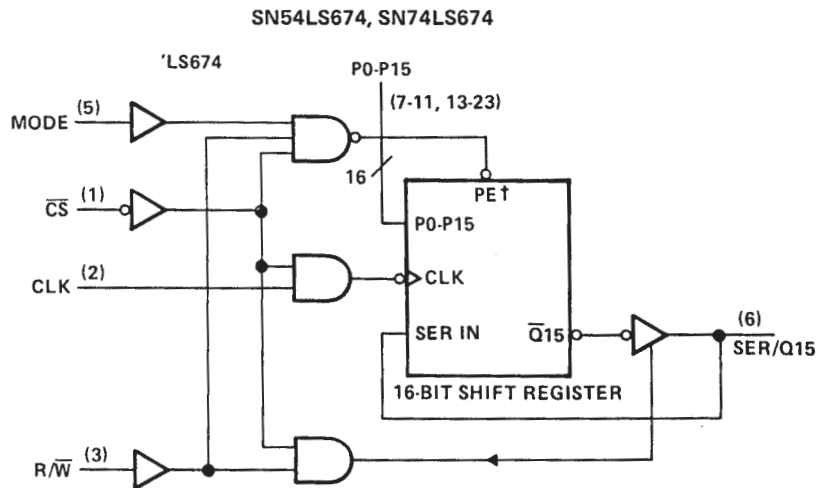
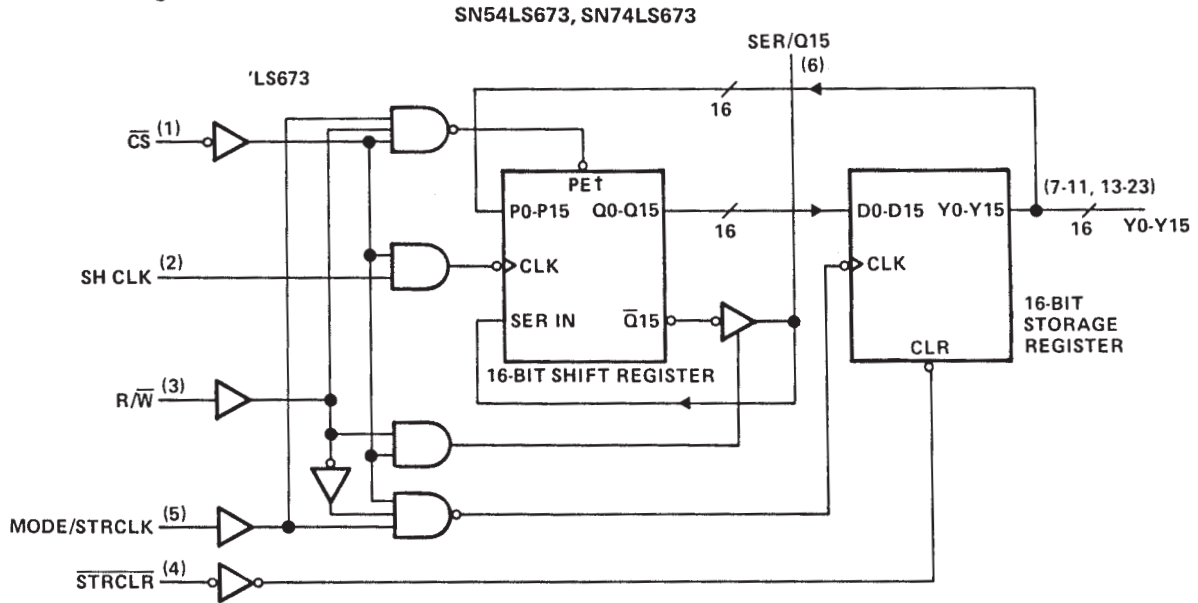


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

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## functional block diagrams

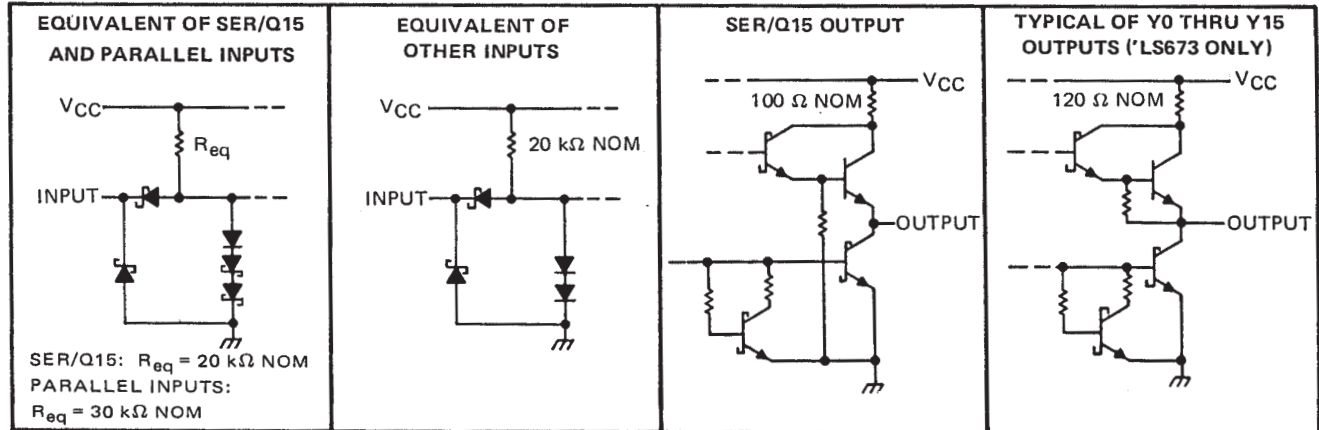


†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

# SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: SER/Q15	5.5 V
All others	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674	-55°C to 125°C
SN74LS673, SN74LS674	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$	High-level output current	SER/Q15		-1	Y0 thru Y15		-2.6	mA
		Y0 thru Y15		-0.4	Y0 thru Y15		-0.4	
$I_{OL}$	Low-level output current	SER/Q15		12	Y0 thru Y15		24	mA
		Y0 thru Y15		4	Y0 thru Y15		8	
$f_{clock}$	Clock frequency	0		20	0		20	MHz
$t_{w(clock)}$	Width of clock input pulse	20			20			ns
$t_{w(clear)}$	Width of clear input pulse	20			20			ns
$t_{su}$	Setup time	SER/Q15		20	Y0 thru Y15		20	ns
		P0 thru P15		20	Y0 thru Y15		20	
		Mode		35	Y0 thru Y15		35	
		$R/\overline{W}$ , $\overline{CS}$		35	Y0 thru Y15		35	
		SH CLK ↓ to Mode/STR CLK ↑ See Note 2		25	Y0 thru Y15		25	
$t_h$	Hold time	SER/Q15		0	Y0 thru Y15		0	ns
		P0 thru P15	'LS673	0	Y0 thru Y15	0		
			'LS674	5.0		5.0		
Mode		0		0				
$T_A$	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.



# SN54LS673, SN54LS674, SN74LS673, SN74LS674

## 16-BIT SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT
			MIN	TYP‡	MAX	MIN	
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.7		0.8	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5		-1.5	V
V <sub>OH</sub>	High-level output voltage	SER/Q15	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,		2.4	3.1	V
		Y0 thru Y15¶	V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = MAX		2.5	3.4	
V <sub>OL</sub>	Low-level output voltage	SER/Q15	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 12 mA	0.25	0.4	V
				I <sub>OL</sub> = 24 mA		0.35	
		Y0 thru Y15¶	V <sub>IL</sub> = V <sub>ILmax</sub>	I <sub>OL</sub> = 4 mA	0.25	0.4	
				I <sub>OL</sub> = 8 mA		0.35	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	SER/Q15	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , V <sub>O</sub> = 2.7 V	40		40	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	SER/Q15	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , V <sub>O</sub> = 0.4 V	-0.4		-0.4	mA
I <sub>I</sub>	Input current at maximum input voltage	SER/Q15	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V		0.1	mA
		Others		V <sub>I</sub> = 7 V		0.1	
I <sub>IH</sub>	High-level input current	SER/Q15	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			40	μA
		Others				20	
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4	mA
I <sub>OS</sub>	Short-circuit output current§	SER/Q15	V <sub>CC</sub> = MAX		-30	-130	mA
		Y0 thru Y15¶			-20	-100	
I <sub>CC</sub>	Supply current	'LS673	V <sub>CC</sub> = MAX		50	80	mA
		'LS674			25	40	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, see note 2

PARAMETER	'LS673		'LS674		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FROM	TO	FROM	TO					
f <sub>max</sub>	SH CLK	SER/Q15	CLK	SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF	20	28		MHz
t <sub>PHL</sub>	STRCLR	Y0 thru Y15			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		25	40	ns
t <sub>PLH</sub>	MODE/ STRCLK	Y0 thru Y15					28	45	
t <sub>PHL</sub>					R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		30	45	ns
t <sub>PLH</sub>	SH CLK	SER/Q15	CLK	SER/Q15			21	33	
t <sub>PZH</sub>	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF		30	45	ns
t <sub>PZL</sub>							30	45	
t <sub>PHZ</sub>	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF		25	40	ns
t <sub>PLZ</sub>							25	40	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
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Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-88602013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SN54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SN54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS674DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
						no Sb/Br)		
SN74LS674DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

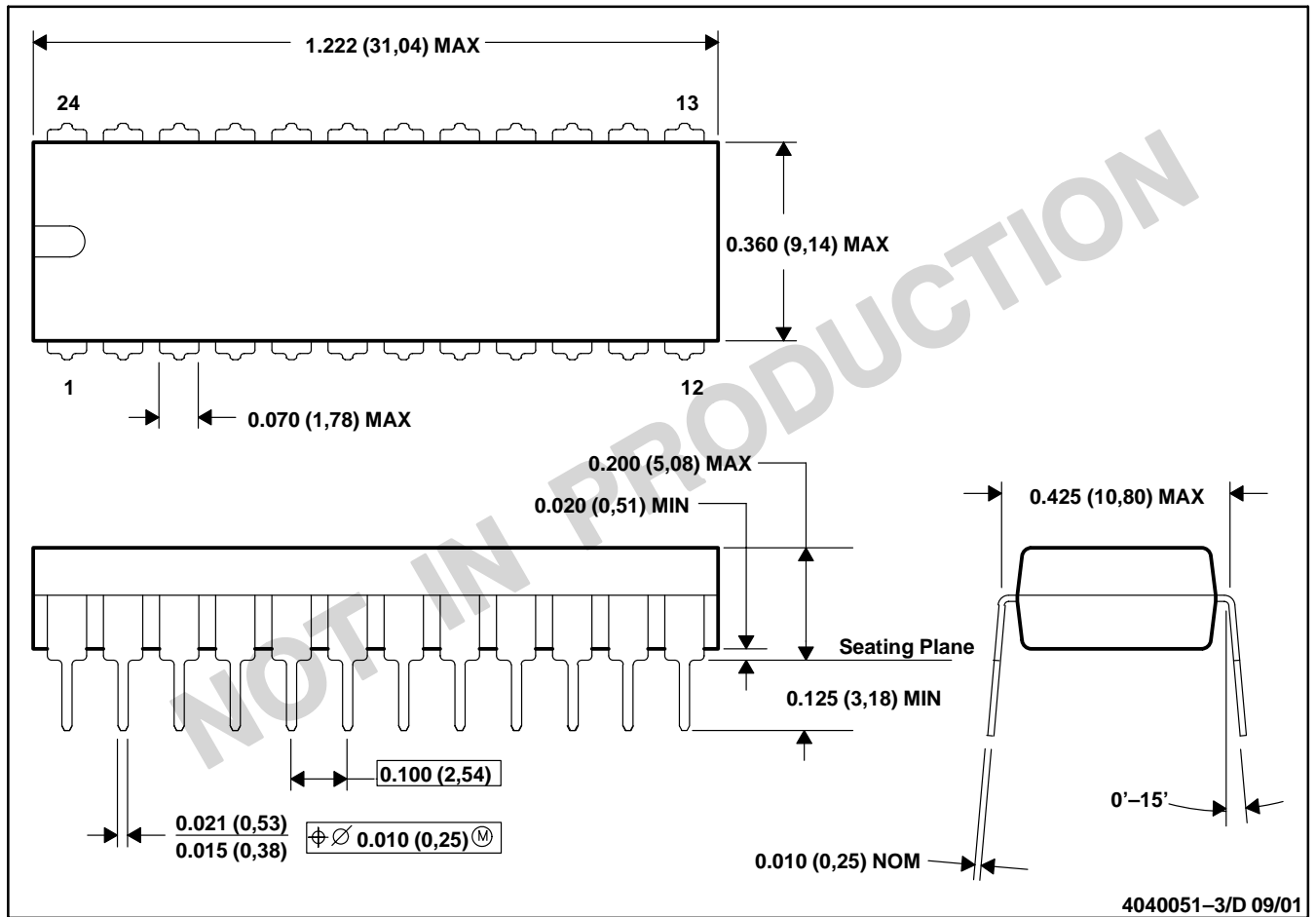
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N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-010



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

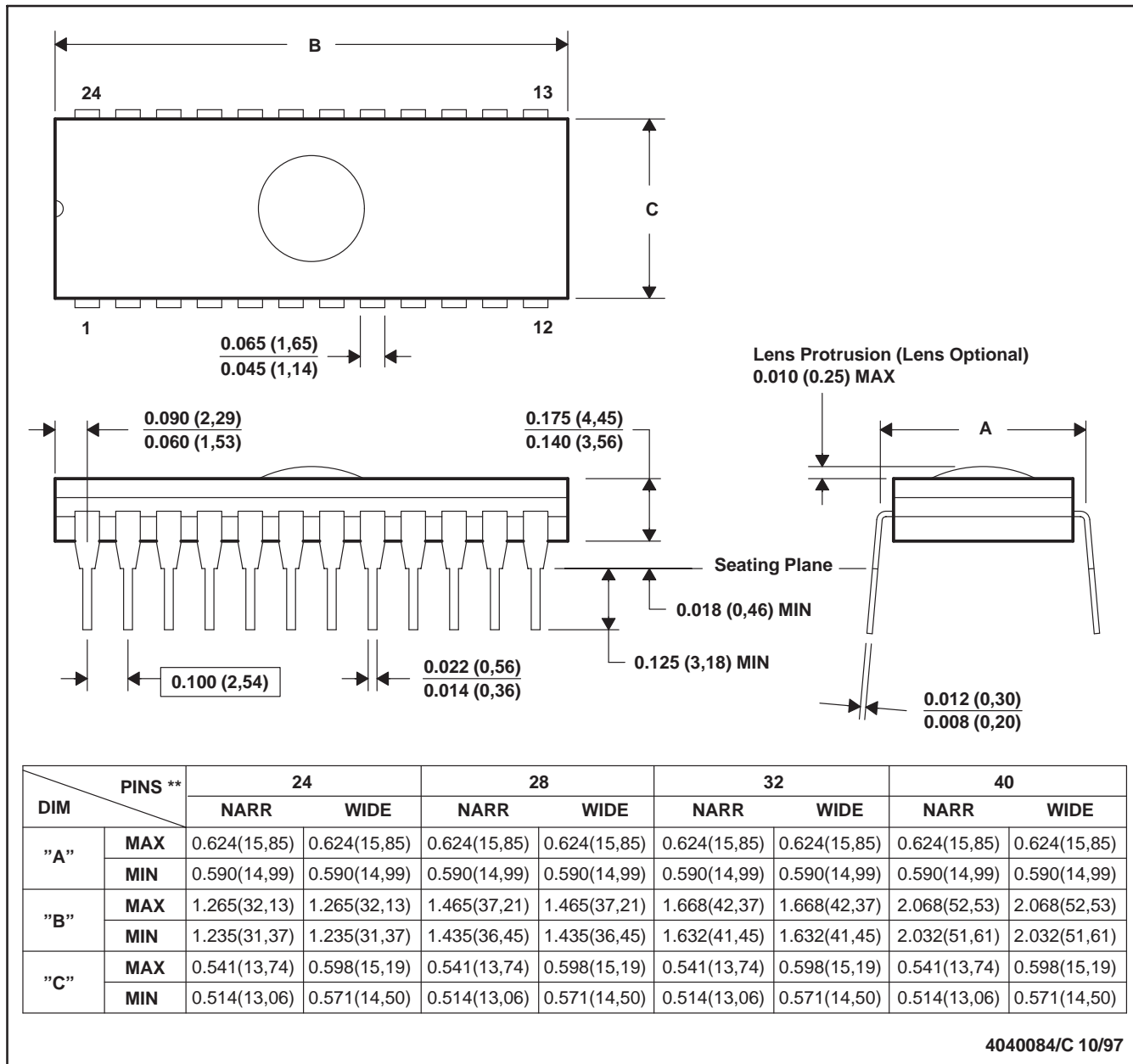


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

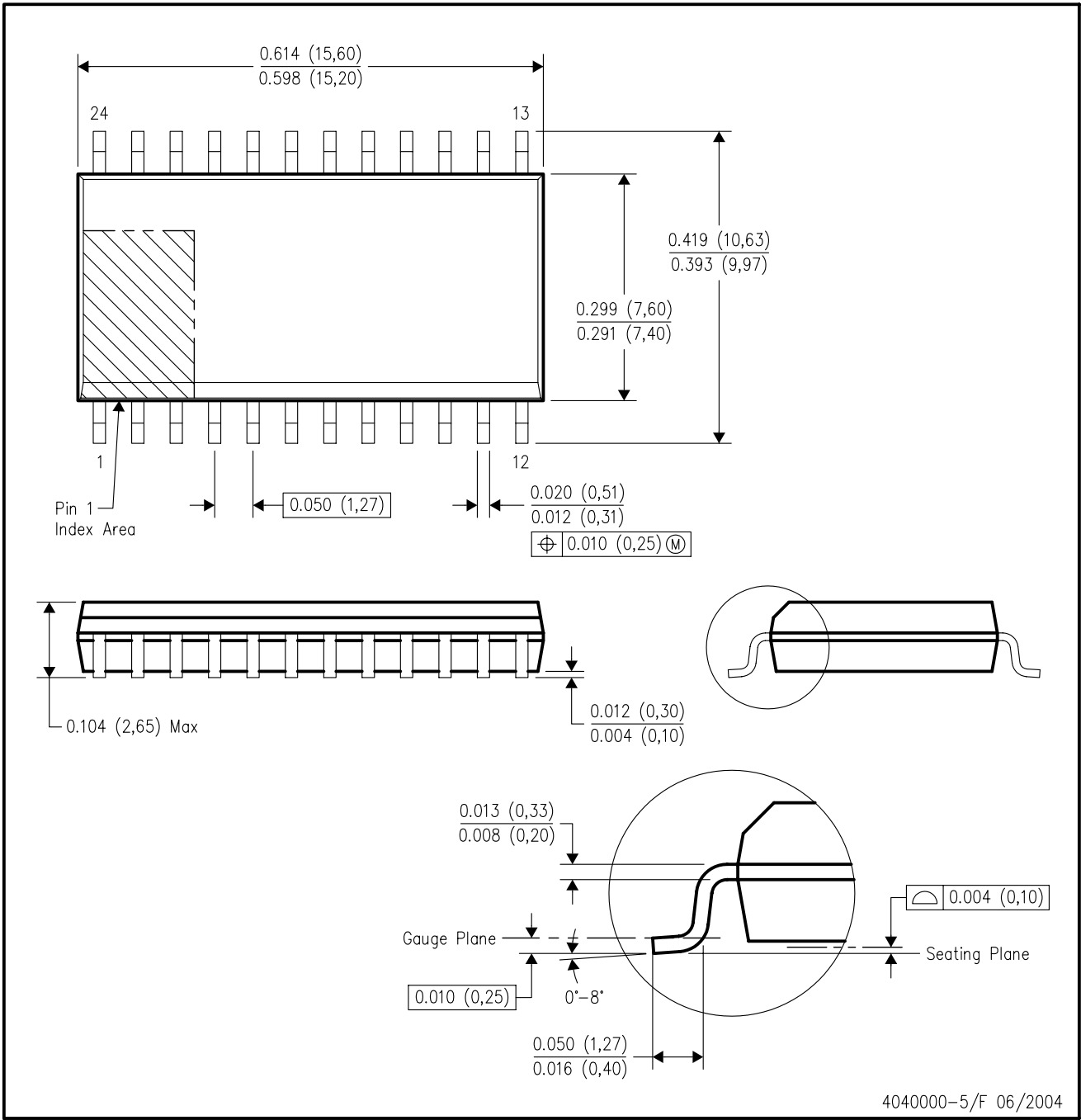
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

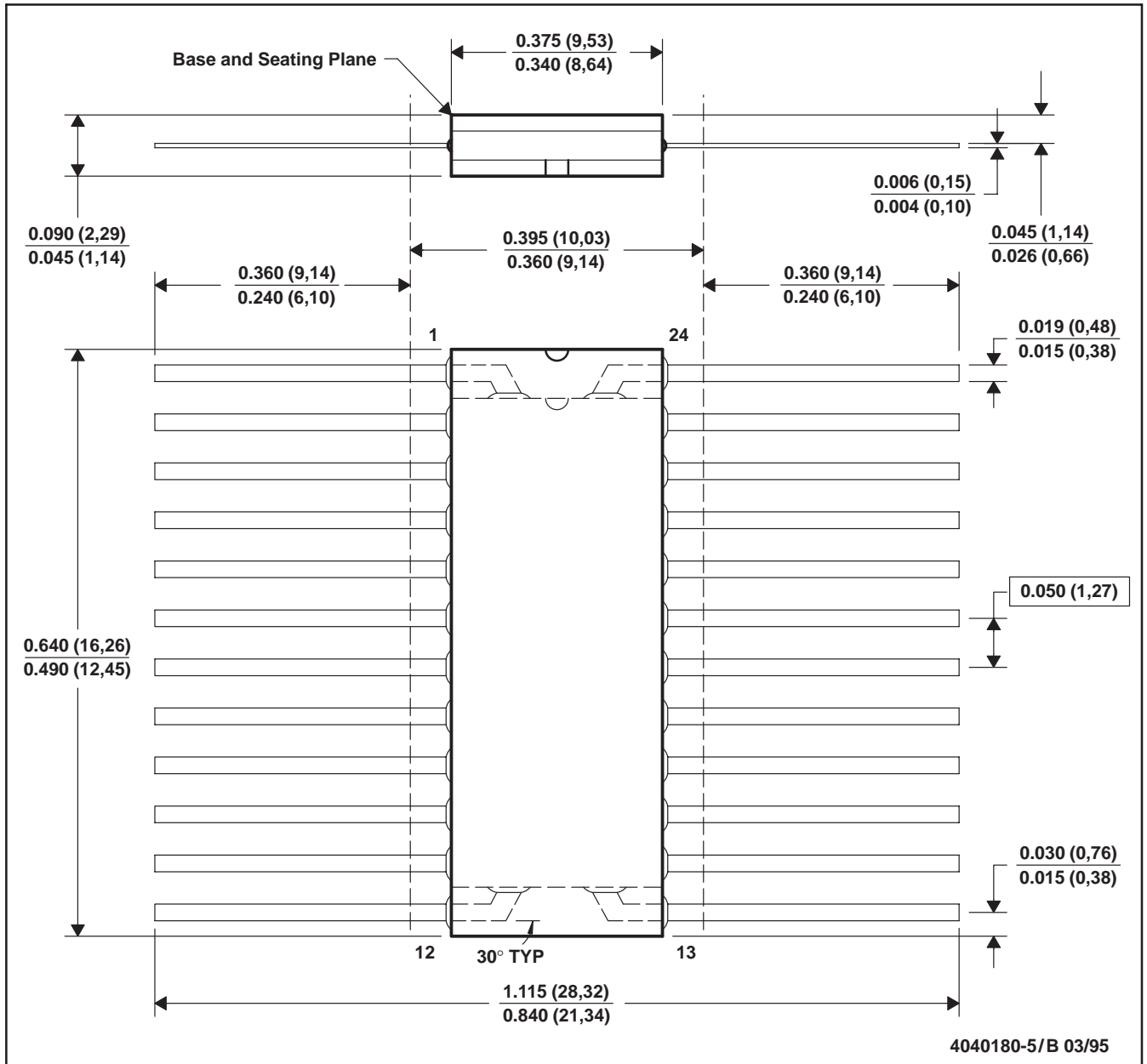


4040053/B 04/95

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD  
 E. Index point is provided on cap for terminal identification only.

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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